REMARKS

The foregoing amendment is to impart greater clarity to the claims rather than to avoid prior art.

Applicants respectfully request reconsideration of this application as amended. Claims 1-29 are pending in the application. Claims 1-29 are rejected. Claims 1 and 5 are amended.

Rejections under 35 U.S.C. 101

Claims 1-8 and 10-18 are rejected under 35 U.S.C. § 101, as allegedly being directed to non-statutory subject matter. Applicant respectfully disagrees.

Claim 1, for example, sets forth:

> 1. (Currently Amended) A method comprising:
> decoding a first shuffle instruction and a first multiply-add instruction, each of an instruction format comprising a first operand field and a second operand field;
> responsive at least in part to said first shuffle instruction, generating a first packed data having a first plurality of byte data elements including an a_1 byte data element, and at least two copies of each of a_2, a_3, and a_4 byte data elements; and
> responsive to said first multiply-add instruction, wherein the first operand field of said first multiply-add instruction specifies said first packed data and the second operand field specifies a second packed data having a second plurality of byte data elements including at least two copies of each of b_1 and b_2 byte data elements, performing an operation $(a_1 \times b_1) + (a_2 \times b_2)$ to generate a first 16-bit data element of a third packed data, performing an operation $(a_2 \times b_1) + (a_3 \times b_2)$ to generate a second 16-bit data element of the third packed data, and performing an operation $(a_3 \times b_1) + (a_4 \times b_2)$ to generate a third 16-bit data element of the third packed data.

An analysis of the instant claims must be performed in order to make a determination of whether the subject matter is statutory. Such analysis should correlate

each claim element with corresponding structures, materials or acts set forth in the specification.

The Federal Circuit makes it clear that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. "The person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips v. AWH Corp.*, 415 F.3d at 1313.

Applicant respectfully submits that in the context of the entire patent, the claimed generating of a packed data having a first plurality of byte data elements including an a_1 byte data element, and at least two copies of each of a_2, a_3, and a_4 byte data elements responsive to a shuffle instruction, and performing operations $(a_1 \times b_1) + (a_2 \times b_2)$, $(a_2 \times b_1) + (a_3 \times b_2)$, and $(a_3 \times b_1) + (a_4 \times b_2)$ to generate 16-bit data elements responsive to a multiply-add instruction, as set forth in claim 1, would be recognized to have practical applications in the technical arts by a person of skill in the art of decompression and display of images and video.

The instant language when correlated with the corresponding structures and processes set forth in the specification (e.g. Figs. 12, 13a-c, 14a-b, 15a-b and 16a-b; pars. 4-5, 26-29, and 142-161) makes it apparent to one of skill in the art that the claimed invention has a practical applications in the technical arts, i.e. efficient bi-linear interpolation and motion compensation of content data for decompression of images and video. Thus, such practical applications in the technical arts include but are not limited to fractional-pixel chrominance motion compensation in accordance with the H.264 standard proposed by the Joint Video Team of the International Telecommunication Union (ITU) Video Coding Experts Group (VCEG) and the International Organization for Standardization/International Electrotechnical Commission (ISO/IEC) Motion Picture

Experts Group (MPEG) for decompression and display of images and video, which are representative of or constitute physical activity or objects.

In addition, Applicant respectfully submits, that the present application clearly asserts such a practical application in the technical arts.

For example, paragraph 4 of the specification (emphasis added) asserts that:

> Accordingly, the display of images, as well as playback of audio and video data, which is collectively referred to herein as content, have become increasingly popular applications for current computing devices. Bi-linear interpolation and motion compensation are popular techniques for decompression and display of images and video. Quarter-pixel and eighth-pixel motion compensation of luminance content in prior decompression techniques have made use of Finite Impulse Response (FIR) filters for interpolation. However for fractional-pixel chrominance motion compensation, bi-linear interpolation may be used instead.

Paragraph 5 of the specification (emphasis added) asserts that:

> Recently bi-linear interpolations have been proposed by the Joint Video Team of the International Telecommunication Union (ITU) Video Coding Experts Group (VCEG) and the International Organization for Standardization/International Electrotechnical Commission (ISO/IEC) Motion Picture Experts Group (MPEG) for fractional-pixel chrominance motion compensation in accordance with the H.264 standard (see Final Committee Draft of ISO/IEC 14496-10 Advanced Video Coding). Although the number of chrominance components is typically only half of the number of luminance components, the processing required for motion compensation of both types of components may be substantially equal.

Paragraph 26 of the specification (emphasis added) asserts that:

> A method and apparatus for efficient bi-linear interpolation and motion compensation of content data are described. In one embodiment, two or more lines of 2n+1 content byte elements may be shuffled to generate a first and second packed data respectively including at least a first and a second 4n byte elements including 2n-1 duplicated elements. A third packed data including sums of products is generated from the first packed data and packed byte coefficients by a multiply-add instruction. A fourth packed data including sums of products is generated from the second packed data and elements and packed byte coefficients by another multiply-add instruction. Corresponding sums of products of the third and fourth packed data are then summed, and may be rounded and averaged.

Paragraph 29 of the specification (emphasis added) asserts that:

> In one embodiment, methods of the present invention are embodied in machine-executable instructions. The instructions can be used to cause a general-purpose or special-purpose processor that is programmed with the instructions to perform the steps of the method. Alternatively, the steps of the method might be performed by specific hardware components that contain hardwired logic for performing the steps, or by any combination of programmed computer components and custom hardware components.

Paragraph 142 of the specification (emphasis added) asserts that:

> **Figure 12** illustrates one exemplary embodiment of a bi-linear interpolation and motion compensation of content data. Figure 12 illustrates a first line of 2n+1 bytes (a, b, c, d and e) and a second line of 2n+1 bytes (f, g, h, i, and j). Bi-linear interpolation and motion compensation may be performed, for example at quarter-pixel or eighth-pixel luminance resolution, on sub-sampled chrominance values to obtain 2n interpolated values (A, B, C and D).

Paragraph 144 of the specification (emphasis added) also asserts that:

> Bi-linear interpolations have been proposed by the Joint Video Team of the International Telecommunication Union (ITU) Video Coding Experts Group (VCEG) and the International Organization for Standardization/International Electrotechnical Commission (ISO/IEC) Motion Picture Experts Group (MPEG) for fractional-pixel chrominance motion compensation in accordance with the H.264 standard (see Final Committee Draft of ISO/IEC 14496-10 Advanced Video Coding). It will be appreciated that bi-linear interpolation may be broadly useful in many other image processing or video processing applications. Especially in applications where small integer data types are used and have sufficient representational range, the techniques detailed below may also be found useful.

Thus the specification makes it readily apparent to one of skill in the art that the claimed invention has practical applications in the technical arts of transforming or reducing video and image data or digital signals representative of or constituting physical activity such as sporting events, news, weather or objects such as products, streets, buildings, animals, humans, etc. to a different state or thing.

The Supreme Court held that the focus in any statutory subject matter analysis be on the claim as a whole, stating "When a claim containing a mathematical formula implements or applies that formula in a structure or process which, when considered as a whole, is performing a function which the patent laws were designed to protect (e.g.,

transforming or reducing an article to a different state or thing, then the claim satisfies the requirements of § 101." *In re Alappat*, 33 F.3d 1526, 1543 (Fed. Cir. 1994) (quoting *Diehr*, 450 U.S. at 192, 209 USPQ at 10).

This notion is sometimes phrased in terms of requiring a transformation or reduction of 'subject matter.' In Schrader, the phrase 'subject matter' was determined not to be limited to tangible articles or objects, but includes intangible subject matter, such as data or signals, representative of or constituting physical activity or objects. *Schrader*, 22 F.3d at 295, 30 USPQ2D (BNA) at 1459.

Thus Applicant respectfully submits that Claims 1-8 and 10-12 are directed to statutory subject matter.

Rejections under 35 U.S.C. 112

Claims 1-29 stand rejected under 35 USC § 112, second paragraph, as allegedly being indefinite for failing to point out and distinctly claim the invention. Applicant respectfully disagrees.

The issue of definiteness is whether, in light of the teachings of the prior art and of the particular invention, the claims set out and circumscribe a particular area with a reasonable degree of precision and particularity. *In re Moore*, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971).

Claim 13, for example, sets forth:

> 13. (Original) A machine-accessible medium including data that, when accessed by one or more machines, causes said one or more machines to:
>
> shuffle a first 2n+1 byte elements of a first line of data to generate a first packed data comprising at least a first 4n byte elements including 2n-1 duplicated elements of the first 2n+1 byte elements;
>
> shuffle a second 2n+1 byte elements of a second line of data to generate a second packed data comprising at least a second 4n byte elements including 2n-1 duplicated elements of the second 2n+1 byte elements;
>
> multiply-add the first packed data with at least a first two byte coefficients to generated a third packed data including sums of products;

multiply-add the second packed data with at least a second two byte coefficients to generated a fourth packed data including sums of products; and

add corresponding sums of products of the third and fourth packed data to generate a first packed result.

The test for definiteness under 35 U.S.C. § 112 is whether those skilled in the art would understand what is claimed when the claim is read in light of the specification. *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d, 1081, 1088 (Fed. Cir. 1986).

Applicant respectfully submits that the specification has set forth a full and clear description of the claimed subject matter. For example, paragraph 26 of the specification (emphasis added) discloses that:

> A method and apparatus for efficient bi-linear interpolation and motion compensation of content data are described. In one embodiment, two or more lines of 2n+1 content byte elements may be shuffled to generate a first and second packed data respectively including at least a first and a second 4n byte elements including 2n-1 duplicated elements. A third packed data including sums of products is generated from the first packed data and packed byte coefficients by a multiply-add instruction. A fourth packed data including sums of products is generated from the second packed data and elements and packed byte coefficients by another multiply-add instruction. Corresponding sums of products of the third and fourth packed data are then summed, and may be rounded and averaged.

Paragraph 66 of the specification (emphasis added) discloses that:

> **Figure 4a** illustrates packed data-types according to one embodiment of the invention. Three packed data formats are illustrated; packed byte 411, packed word 412, and packed doubleword 413. Packed byte, in one embodiment of the invention, is sixty-four bits long containing eight data elements. In an alternative embodiment, packed byte may be sixty-four or one hundred twenty-eight bits long containing eight or sixteen data elements. Each data element is one byte long. Generally, a data element is an individual piece of data that is stored in a single register (or memory location) with other data elements of the same length. In one embodiment of the invention, the number of data elements stored in a register is sixty-four bits or one hundred twenty-eight bits divided by the length in bits of a data element.

Paragraph 108 of the specification (emphasis added) also discloses that:

> While in some specific examples, packed data sources and destinations may be represented as having 64-bits, it will be appreciated that the principals

disclosed herein may be extended to other conveniently selected lengths, such as 80-bits, 128-bits or 256-bits.

Paragraph 142 of the specification further illustrates an example of a bi-linear interpolation and motion compensation (emphasis added) disclosing that:

> **Figure 12** illustrates one exemplary embodiment of a bi-linear interpolation and motion compensation of content data. Figure 12 illustrates a first line of 2n+1 bytes (a, b, c, d and e) and a second line of 2n+1 bytes (f, g, h, i, and j). Bi-linear interpolation and motion compensation may be performed, for example at quarter-pixel or eighth-pixel luminance resolution, on sub-sampled chrominance values to obtain 2n interpolated values (A, B, C and D).

Applicant respectfully submits that at least in light of the above disclosure set forth by the specification, the claims set out and circumscribe shuffling 2n+1 byte elements of first and second lines of data to generate first and second packed data each comprising at least 4n byte elements including 2n-1 duplicated elements of the first 2n+1 byte elements with a reasonable degree of precision and particularity.

See also, for example, Figure 14a, and paragraph 150, which discloses that:

> In processing block 1401, a line 1410 with 2n+1 byte elements stored in SRC1 is shuffled according to according to packed data 1460 stored in SRC2 to generate Result 1411 comprising a first 4n byte elements.

and paragraph 151, which discloses that:

> In processing block 1402 a line 1420 with 2n+1 byte elements stored in SRC1 is shuffled according to according to packed data 1460 stored in SRC2to generate Result 1421 comprising a second 4n byte elements.

Applicant also submits with regard to Claim 13, that Claim 18 further sets forth (emphasis added):

> 18. (Original) The machine-accessible medium of Claim 17 wherein n is equal to 2 ...

and with regard to Claim 19, that Claim 20 further sets forth (emphasis added):

> 20. (Original) The apparatus of Claim 20 wherein n is at least two.

and with regard to Claim 25, that Claims 26 and 27 further set forth (emphasis added):

26. (Original) The computing system of Claim 25 wherein each of the first, second, third and fourth packed data comprise 16 byte data elements.

27. (Original) The computing system of Claim 25 wherein each of the first, second, third and fourth packed data comprise 8 byte data elements.

With regard to Claim 17, the Examiner is respectfully directed to Figure 14a (1402 and 1403) and to paragraphs 151-152, for example, which state:

> In processing block 1402 a line 1420 with 2n+1 byte elements stored in SRC1 is shuffled according to according to packed data 1460 stored in SRC2to generate Result 1421 comprising a second 4n byte elements… In processing block 1403, Result 1411 comprising a first 4n byte elements and Result 1421 comprising a second 4n byte elements are unpacked, …to generate Result 1612.

The Examiner is also directed to Figure 14b (1404 and 1405) and to paragraphs 153-154, for example, which state:

> In processing block 1404 a line 1430 with 2n+1 byte elements stored in SRC1 is shuffled according to according to packed data 1460 stored in SRC2to generate Result 1431 comprising a third 4n byte elements… In processing block 1405, Result 1421 comprising the second 4n byte elements and Result 1431 comprising the third 4n byte elements are unpacked, … to generate Result 1622.

Thus Applicant respectfully submits that one skilled in the art would understand that Claim 17 is consistent with lines 6-8 of Claim 13, at least when Claim 17 is read in light of the disclosure set forth by the specification.

With regard to Claim 18, the Examiner is respectfully directed to Figure 13c (1336 and 1337), Figure 16b (1604 and 1605) and to paragraph 60, for example, which states:

> In processing block 1604, rounding is optionally applied to the 4n sums of Result 1611 by adding rounding values ($s^2/2$) from packed data 1660 at the desired bit positions of the elements of Result 1611 to generate Result 1613. In processing block 1605, Result 1614 comprising 4n packed averages over an area (s^2) is computed from the 4n packed sums of Result 1613 by shifting the elements of Result 1613 by a shift count substantially equal to the log (base 2) of the area (i.e. $\log_2(s^2)$).

Since Claim 13 sets forth generating a first packed result, and since Claim 18 sets forth a second packed result comprising at least 4n rounded averages, each corresponding

to an element of said first packed result, one skilled in the art would understand how Claim 18 is related to the previous steps, at least when it is read in light of the disclosure set forth by the specification.

Thus, Applicant respectfully submits that one skilled in the art would understand what is claimed when the claim is read in light of the specification. Accordingly, Applicant submits that that in light of the specification, the claims set out and circumscribe the claimed subject matter with a reasonable degree of precision and particularity required by 35 USC § 112, second paragraph.

CONCLUSION

Applicants respectfully submit the amended specification, and the present claims for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence Mennemeier at (408) 765-2194.

Authorization is hereby given to charge our Deposit Account No. 50-0221 for any charges that may be due.

Respectfully submitted,

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